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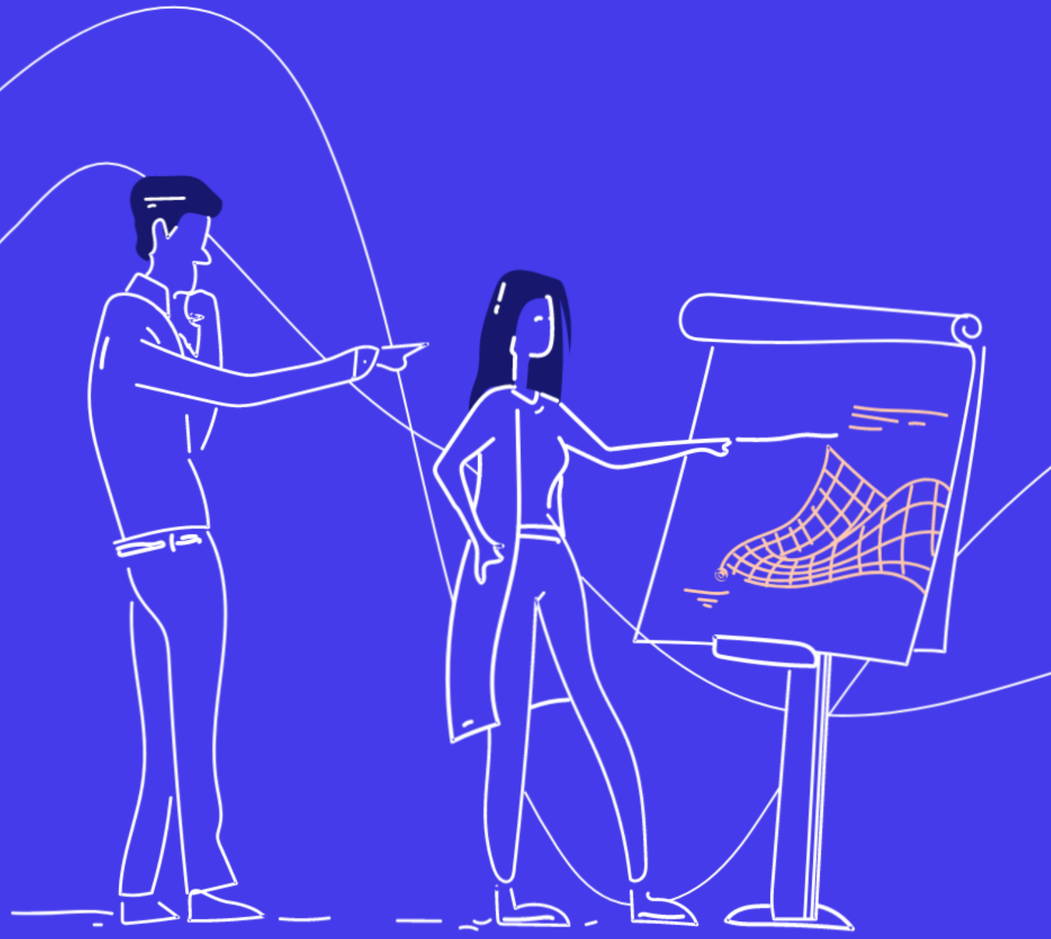
Programming Zynq RF SoCs Using Simulink



SciEngineer’s training courses are designed to help organizations and individuals close skills gaps, keep up-to-date with the industry-accepted best practices and achieve the greatest value from MathWorks® and COMSOL® Products.

Programming Zynq RF SoCs Using Simulink

This hands-on, two-day course focuses on developing and configuring models in Simulink® and deploying on Xilinx® Zynq® UltraScale+ RFSoCs.

Prerequisites

Programming Xilinx® Zynq® SoCs with MATLAB® and Simulink. Knowledge of concepts of communication systems and hardware design.

TOPICS

Day 1

- RFSoC Device Overview
- Frequency Planning
- Getting the model ready for the RFSoC

Day 2

- Target RFSoC using SoC Blockset
- Hardware Software Co-design for RFSoC

RFSoC Device Overview

OBJECTIVE: Introduction to RFSoC's device settings, parameters, and hardware details.

- Introducing Zynq RFSoC.
- Reviewing RFSoC transceiver tiles.
- Examining RFSoc digital up converter and down converter.
- Reviewing differences between RFSoC Generation 1 and Generation 3 devices.
- Reviewing the support offerings of MathWorks (R) for RFSoC

Frequency Planning

OBJECTIVE: Provide an introduction to frequency planning with Nyquist zones and sampling rates as used with the DAC and ADC tiles in the RFSoC.

- Using the DAC tile Digital Quadrature Modulator for digital up conversion
- Using the normal mode (Nyquist Zone 1) and mixed mode (Nyquist Zone 2) operations of DAC tiles for transmission
- Applying a bandpass sampling theorem to choose a sampling rate for the receive

Getting the model ready for the RFSoC

OBJECTIVE: Simulate transmission and reception of a digital signal in the RFSoC.

- Review frame-based processing
- Simulate a transmitter and receiver model for the RFSoC
- Prepare model for deployment to the RFSoC

Target RFSoC using SoC Blockset

OBJECTIVE: Simulate, model and perform analysis of SoC HW/SW architectures specifically to target gen 1,3 RFSoC.

- Introduction to SoC Blockset
- Use RFSoC template from SoC Blockset to create RFSoC system modeling framework
- Simulate and generate code for PL and PS side of algorithm using SoC Builder
- Deploy application on the board targeting FPGA, ARM and RF converter tiles

Hardware Software Co-design for RFSoC

OBJECTIVE: Deploy and interact with your HDL IP design at run-time verify performance from MATLAB.

- Generate and examine the RFSoC Vivado project
- Access streaming and parameter data of the generated HDL IP at run-time
- Dynamically configure RF Data Converter settings in MATLAB

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